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"Circuit arrangement for DC-isolated signal transmission"

The invention relates to a circuit arrangement for DC-isolated transmission of an analog input variable by means of a signal transformation part, having a voltage input and a voltage output, and in particular also for voltage matching between the voltage input and the voltage output of the circuit arrangement.

Circuit arrangements of this type are used in industry for the transmission of control signals in devices having an analog signal control input for 0 to 10 volts. Circuit arrangements of this type are also used for example for desired value setting of a regulator or for evaluation of a process variable in a control loop.

Owing to existing safety standards, a control signal must be DC-isolated from a power supply system and be accessible in the sense of these safety standards. An electric circuit of this type is referred to as an SELV or PELV electric circuit.

Circuit arrangements are known which satisfy this requirement by converting the analog signal, with an auxiliary energy being fed in, in such a way that the signal can be transmitted with the aid of simple optoelectronic elements, e.g. optocouplers and the DC isolation can thereby be achieved. This requires in some instances a relatively complicated conversion of the analog signal into a pulse-width-modulated square-wave signal, and vice versa, because simple

optocouplers are only suitable for digital signals. Moreover, in a manner governed by the system, solutions of this type are not linear in the range around 0V or 10V input voltage. Although linear optocouplers with which an analog-to-digital conversion and vice versa is obviated are also known, they are expensive and generally have to be adjusted.

Another problem is also posed by different voltage ranges that are required for different assemblies or circuits. Whereas a 0 to 10 volt signal is industry standard e.g. for a desired value setting in a control loop, a microcontroller requires an input voltage range of e.g. 0 to 5 volts. This conversion has to be as free from errors as possible, i.e. the signal transmission has to be effected with the greatest possible linearity.

The invention is based on the object of providing a circuit arrangement of the type mentioned in the introduction which is highly linear and enables a DC signal isolation in a simple manner.

This object is achieved by virtue of the fact that the signal transformation part is designed as an inductive signal transformation part and the circuit arrangement is provided with a charging and discharging arrangement having a switching element in such a way that, as a result of the switching element being actuated, a charging or discharging current that is proportional to an input voltage and flows through the signal transformation part occurs and an output voltage is established at the voltage output.

It is advantageous if the inductive energy store contained in the signal transformation part is constructed with a core made of magnetizable material and a first (primary, number of turns n1) and second

(secondary, number of turns n2) winding with the turns ratio ü = n1/n2.

The invention actually makes it possible to use an inductive signal transformation part, which is constructed e.g. like an AC transformer for the transmission of electrical energy, for the transmission of an arbitrary analog control signal (i.e. also of a DC voltage) in a simple manner without auxiliary energy being fed in on the input side.

Hitherto, transformers have been used e.g. for DC-isolated energy transmission with sinusoidal currents or other periodic alternating currents.

A further development thereof is clocked energy transmission systems such as e.g. switch-mode power supplies. The side effects that occur in this case are utilized by the invention described here.

Currents and voltages at the transformer are related here too by the turns ratio ü and can be measured at the primary and also at the secondary in the event of flux changes in the core. Thus, e.g. in the case of an inhibited primary current flow and a secondary-side demagnetization process, it is possible to measure a "mapping" of the secondary voltage at the primary winding.

In order to generate a magnetic flux in the core, the transformer in the signal transformation part is connected up to a switching element in such a way that the primary winding of the transformer is connected to voltage in the form of a temporally limited sampling, as a result of which a primary-side current flow can be generated. A magnetization of the core is thereby achieved. Immediately after the switching element is switched off, the primary-side current flow is

interrupted, as a result of which the magnetization is terminated, which leads to a current flow (as conservation variable at the transformer) in the ratio ü in the secondary winding, which then brings about the demagnetization of the core. The driving variable for the demagnetization current is the output voltage of the transformer, which can be measured as a "reflected" mapping on the primary side of the transformer.

In order to realize the demagnetization current flow, a smoothing capacitor is preferably connected on the secondary side of the transformer, which smoothing capacitor is charged firstly by the control voltage fed in on this side and secondly by the energy transmitted via the transformer. A discharge resistor connected in parallel brings about a continuous discharging of the capacitor by the magnitude by which it was charged by the quantity of energy transmitted via the core per sampling process. This prevents a further and further rise in the voltage at the capacitor.

At the same time, a voltage divider connected upstream of the inductive signal transformation part is formed by an input-side resistor that forms a series circuit with the discharge resistor. Selection of identical resistors and a turns ratio of the transformer of ü = 1 result in signal matching that reduces the 0-10 V input signal to the 0-5 V input of components connected downstream such as e.g. of a microcontroller. This matching must be effected as precisely as possible and as linearly as possible.

The invention's configuration of the circuit arrangement makes it possible to obviate not only at least one signal conversion circuit, e.g. for an analog-to-digital conversion and vice versa, but also a DC-isolated power supply for the conversion circuit.

The inductive signal transformation part is additionally independent of aging, cost-effective and requires little space, e.g. on a printed circuit board.

In comparison with optoelectronic solutions, the circuit arrangement according to the invention is highly linear and thus has a very low transmission error.

Further advantages of the invention are contained in the subclaims.

The invention and also further advantages thereof are explained in more detail with reference to an exemplary embodiment and the drawing. In this case, identical parts are always identified by the same reference symbols.

In the figures:

figure 1 shows a circuit arrangement according to the invention,

figure 2 shows current and voltage timing diagrams,

figure 3 shows, for comparison, a first known variant of a DC decoupling with a simple optocoupler, and

figure 4 shows, likewise for comparison, a second known variant of a DC decoupling with a linear optocoupler.

Figure 1 shows an exemplary embodiment of a circuit arrangement 1 according to the invention. This circuit arrangement can be used in industry for controlling devices with an analog signal and with a voltage U1 of 0 to 10 volts. It may serve for example for desired

value setting of a regulator or for evaluating a process variable in a control loop. In particular, it is used for rotational speed control of a commutatorless DC motor, a 0 to 10 volt input being present. An output-side voltage matching to 0 to 5 volts (U3) is additionally effected.

The circuit arrangement 1 has a voltage input 4 and a voltage output 5 and comprises two circuit parts 2 and 3 used to achieve a DC isolation, a linear transmission of an analog control variable and, in particular, the voltage matching between the voltage input U1 and the voltage output U3. The two circuit parts 2 and 3 are electrically connected to an inductive signal transformation part 6 such that a first winding W1 of the signal transformation part 6 is assigned to the input-side circuit part 2 and a second winding W2 of the signal transformation part 6 is assigned to the output-side circuit part 3.

The signal transformation part 6 is an inductive energy store and comprises, in a known manner, a closed core made of magnetizable material around which the two windings W1, W2 are arranged, the windings W1 and W2 running in opposite senses or the circuit parts 2, 3 being arranged in corresponding fashion as illustrated by the diagonally offset points at the windings W1, W2.

The input-side circuit part 2 preferably comprises two resistors R1, R2, a smoothing capacitor C1 and a diode D1. In this case, the smoothing capacitor C1 is electrically arranged between the electrical resistor R2 connected in parallel with it and the winding W1 or an inductance TR1 of the signal transformation part 6. Between the capacitor C1 and the winding W1, the diode acting as rectifying element D1 is connected up in the reverse direction with respect to the voltage input. Furthermore, a charging resistor R1 is connected

upstream of the capacitor C1. The resistors R1 and R2 are connected in series and form a voltage divider. The charging resistor R1 is connected directly to the input, so that the input voltage U1 is divided in accordance with the division ratio between the two resistors R1, R2, said division ratio being defined by the resistors R1 and R2. The capacitor C1 is simultaneously a smoothing element and a charging and discharging element.

The output-side circuit part 3 preferably comprises a transistor as switching element S1 and a semiconductor element with differential inputs, which is embodied as a differential amplifier V1. The switching element S1 is connected to a winding end 9 of the signal transformation part 6 by one of its switching ends 7 and to ground or 0 volts by its other switching end 8. The differential amplifier V1 is connected up by its differential inputs to the two winding ends 9, 10 of the signal transformation part 6 that are on the control voltage output side. The output of the differential amplifier V1 forms the voltage output 5 with the output voltage U3.

The elements illustrated in figure 1 are connected according to the invention to form a charging and discharging arrangement which functions as follows:

The analog voltage U1 in the voltage range of 0 to 10 volts is present at the control voltage input 4. The capacitor C1 is charged to a voltage value Uc1, to be precise in accordance with the formula

$$Uc1 = \frac{R2}{R1 + R2} * U1 \qquad (1)$$

In this case, the diode D1 prevents a current from flowing into the winding W1 on account of the voltage

U1 since it is connected in such a way that it assumes a turned-off state during this charging operation. The resistors R1, R2 form a matching circuit part which can be used to alter an output voltage.

The switching element S1 enables a sampling operation. The value stored in the capacitor C1 is sampled in practice by the switching element S1, to be precise preferably from the DC-isolated side.

At the beginning of the sampling operation, the switching element S1 is closed at the instant t0, which is plotted on a time axis t in figure 2.

A current i2 that flows (primary) first through the second winding W2 and the switching element S1 rises until the switching element S1 switches off, to be precise according to the relationship:

$$\frac{di2}{dt} = \frac{Ub}{Lprim} \qquad (2)$$

This ramped current rise of i2 is illustrated in figure 2, in the topmost curve (ramp 15).

Ub is in this case the voltage which is present across the inductance Lprim of the second winding W2 and is a fixed supply voltage of an output-side power supply (not illustrated).

At the instant t1, at which the switching element S1 opens again, a quantity of energy has been stored in the core of the signal transformation part 6, the signal transformation part 6 serving as an inductive energy store. Therefore, a specific quantity of energy is charged in practice into the signal transformation part 6 with the aid of the switching element S1.

This charged quantity of energy amounts to:

$$W = \frac{1}{2} * Lprim(I2, max)^2 \qquad (3)$$

After the switching element S1 has opened, it is necessarily the case that a primary current i2 can no longer flow through the output-side winding W2 with the primary inductance Lprim, so that a secondary current i1 is established on the side of the winding W1, as is shown in the second diagram of figure 2. This effect is based on the fact that the current through the inductance is the conservation variable and is thus driven on by the inductance.

Instead of the current i2, then, the current i1 continues to flow in the secondary winding W2 until the instant t2, at which the core of the signal transformation part 6 is demagnetized and the secondary current i1 has decayed to the value zero.

The following relationship exists in this case:

$$I1,max = ü * I2,max \qquad (4)$$

where ü denotes the turns ratio between the two windings W1 and W2 and i1,max and i2,max denote the currents directly before and directly after the opening instant t1.

The ramped current fall (ramp 16) after the opening instant t1 amounts to:

$$\frac{di1}{dt} = -\frac{Uc1 + Uf}{Lprim * ü^2} \qquad (5)$$

Uc1 is the voltage across the capacitor C1 and Uf is the voltage across the diode D1, which is connected in

the forward direction for this current i1. Uf is constant, e.g. 0.7 volt, in a known manner.

The gradient of the second ramp 16 is dependent on the magnitude of the input voltage U1, as can be seen from equation (1) and equation (5). The voltage U1 in a time window is critical in this case. The time window T1 with a sampling beginning (t0) and a sampling end (t1) is necessary because signal sampling is involved, in principle, the sampled value (U3) being available after the instant t1 in a manner similar to that in the case of a sample & hold circuit (cf. figure 2). The voltage U1 need not be a constant DC voltage, but rather may also change, like any analog control signal. The sampling frequency with which the switching element is driven must be much higher in relation to the possible signal changes of the analog input signal. The sampling frequency may be e.g. 1 Hz to 100 kHz.

However, its value must principally be matched to the magnitude of C1 and R2 since the voltage Uc across the capacitor C1 rises by the amount $\Delta Uc1$ at the same time as the current fall of the current i1 (interval T2 between t1 and t2). By the next sampling that follows, the capacitor C1 must be discharged again by said amount via R2 since the voltage to be measured at the voltage output is otherwise corrupted. The third curve in figure 2 shows the voltage profile at C1.

$\Delta Uc1$ is calculated from:

$$\Delta Uc1 = \sqrt{\frac{Lprim * I2,max^2}{C1}} \qquad (6)$$

In this case, the voltage U2 across the opened switching element S1 is:

$$U2 = ULprim + Ub \qquad (7)$$

As shown in figure 2, fourth curve, U2 is thus higher than Ub in this time interval T2.

ULprim is calculated from:

$$ULprim = ü*(U1 + Uf + \Delta Uc1) \quad (8)$$

It emerges from the abovementioned equations that:

$$U2 = Ub + ü * (\frac{R2}{R1 + R2} * U1 + Uf + \Delta Uc1) \quad (9)$$

If the dimensioning of the inductance Lprim is small enough (or C1 is chosen to be large enough and R2 is chosen to have a sufficiently low resistance) that the voltage increase $\Delta Uc1$ is negligibly small compared with the voltage U1 (cf. equation 6), then the preceding equation 9 is simplified to:

$$U2 = Ub + ü * (\frac{R2}{R1 + R2} * U1 + Uf) \quad (10)$$

This is taken as a basis below.

Through the differential amplifier V1, the following results in the time interval T2 between t1 and t2:

$$U3 = U2 - Ub \quad (11)$$

This results in the following:

$$U3 = ü * (\frac{R2}{R1 + R2} * U1 + Uf) \quad (12)$$

Given ü = 1 and R1 = R2, equation 12 is simplified to:

$$U3 = \frac{1}{2} * U1 + Uf \quad (13)$$

Half the input voltage U1 that is corrupted by the voltage Uf can thus be measured at the output 5 of the differential amplifier V1. However, since the voltage Uf is a fixed variable, the output voltage U3 can be corrected by the known voltage Uf, e.g. 0.7 volt, by suitable means or methods.

As is then apparent, the corrected DC-decoupled output voltage amounts to:

$$U3 = \frac{1}{2} * U1 \qquad (14)$$

Consequently, a DC-isolated output voltage U3 of 0 to 5 volts, given an input voltage U1 of 0 to 10 volts, is present in time-discrete fashion by virtue of the circuit arrangement according to the invention.

Figure 3 shows, for comparison, a first known variant of a DC decoupling with a simple optocoupler 31 (prior art). The input voltage must firstly be digitized by a PWM converter 30 because the optocoupler 31, comprising a transmitter and a receiver, can only transmit digital signals. An integrator 32 must put the signal into analog form again.

Figure 4 shows, likewise for comparison, a second known variant of a DC decoupling with a linear optocoupler 41 with differential amplifiers 40 and 42 (prior art).

An additional DC-isolated power supply is required in both cases (figure 3, figure 4).

The invention is not restricted to the exemplary embodiments illustrated and described, but rather also encompasses all embodiments that are equivalent in the sense of the invention. Furthermore, the invention has

also hitherto still not been restricted to the combination of features defined in claim 1, but rather may also be defined by any arbitrary other combination of specific features of all the individual features disclosed overall. This means that in principle practically any individual feature of claim 1 can be omitted or be replaced by at least one individual feature disclosed elsewhere in the application. In this respect, claim 1 is to be understood merely as a first attempt at formulation for an invention.